The Apple II Cassette Interface (1 of 2)

Revised: 11/20/84
Security: Everyone

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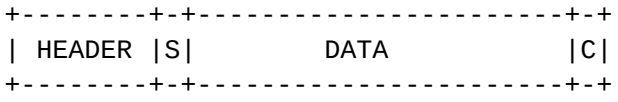
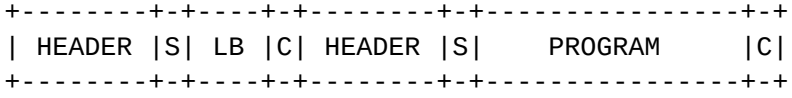
This note is about the cassette interface built into the Apple II and Apple II+, subroutines. An assumption made here is that the cassette recorder is in the proper mode, play or record, when the read and write routines are executed. Note also that the timing is approximate and may vary from one Apple to another.

A record is a block of binary data. This data may be a BASIC or APPLESOFT program, a machine language program, or just binary data. Records representing BASIC or APPLESOFT programs are really two records, the length of the program and the actual program. A record consists of a header, synchronous bit, the actual data, and a checksum byte for error detection.

Monitor record format



BASIC program record format

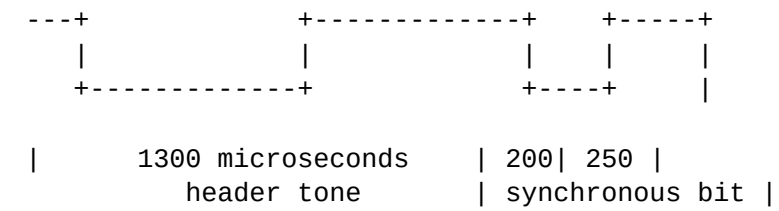


Key: S = SYNC bit
C = CHECKSUM byte
LB = BASIC program length

The header consists of 10 seconds of 770 Hz tone, (1 cycle equals 1300 microseconds). This gives enough time for the cassette motor to attain speed and the plastic tape leader to go by. A subroutine called HEADR generates a shortened header between the BASIC length bytes and the BASIC program itself. The length of the header tone is controlled by the value of the accumulator on entry to the subroutine. This can vary from 0.2 seconds to 40 seconds. On entry the X register should be 0 and the carry flag should be set. HEADR also generates a synchronous bit at the end of the tone. HEADR resides at

hexadecimal address $FCC9, or decimal address -882.

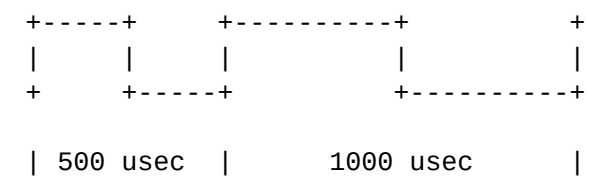
The last cycle of header tone and SYNC bit



The synchronous bit, generated by HEADR, is one half cycle of 2500 Hz, (200 microseconds) and one half cycle of 2000 Hz, (250 microseconds). It is used to signal the end of the header tone and the start of the data.

The data is recorded on the tape with a low starting address and a high ending address. Each byte of data is shifted out most significant bit first, least significant bit last. A zero bit is made up of one cycle of 2 kHz, (250 microseconds per half cycle) and a one bit is one cycle of 1 kHz, (500 microseconds per half cycle). This works out to 2000 baud for zeros only and 1000 baud for ones, or an average of 1500 baud.

A zero bit and a one bit



The checksum byte is written on the tape at the end of the data block. All during reading or writing each data byte is EXCLUSIVE OR-ed with the checksum byte. If the checksum computed during a read agrees with the checksum that was written out, then the data is probably good. This method will detect an odd number of errors for any of the eight bits of the byte.

In writing data, the cassette output uses quite simple circuitry, a flip-flop connected through a voltage divider to the jack on the back panel of the Apple. Any time the address $C020 is accessed this flip-flop changes state. Accessing the flip-flop once every 500 microseconds generates a 1000 Hz tone.

Apple Tech Notes

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