



Data Sheet

Keyboard encoder IC 9600-PRO

RS stock number 633-161

The 9600 is a keyboard encoder that contains all the logic necessary to debounce and encode the SPST key switches used in a keyboard matrix and provide a fully decoded data output consisting of a nine bit simple binary code which can be converted to the required information code by a PROM or microprocessor etc. This permits maximum user flexibility for key layout and coding.

Contact bounce elimination circuitry with an externally controllable delay is included and data outputs are TTL compatible.

Absolute maximum ratings

Positive voltage any pin with respect to Gnd ____ +8.0V

Negative voltage any pin with respect to Gnd ____ 0.3V

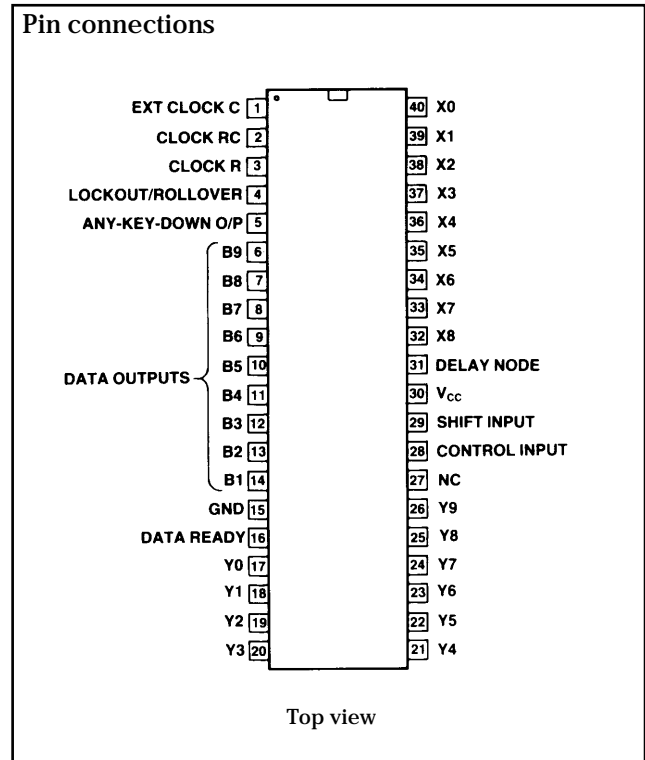
Operating temperature range _____ 0°C to +70°C

Storage temperature range _____ -55°C to +150°C

Lead temperature soldering 10s _____ +325°C

Features

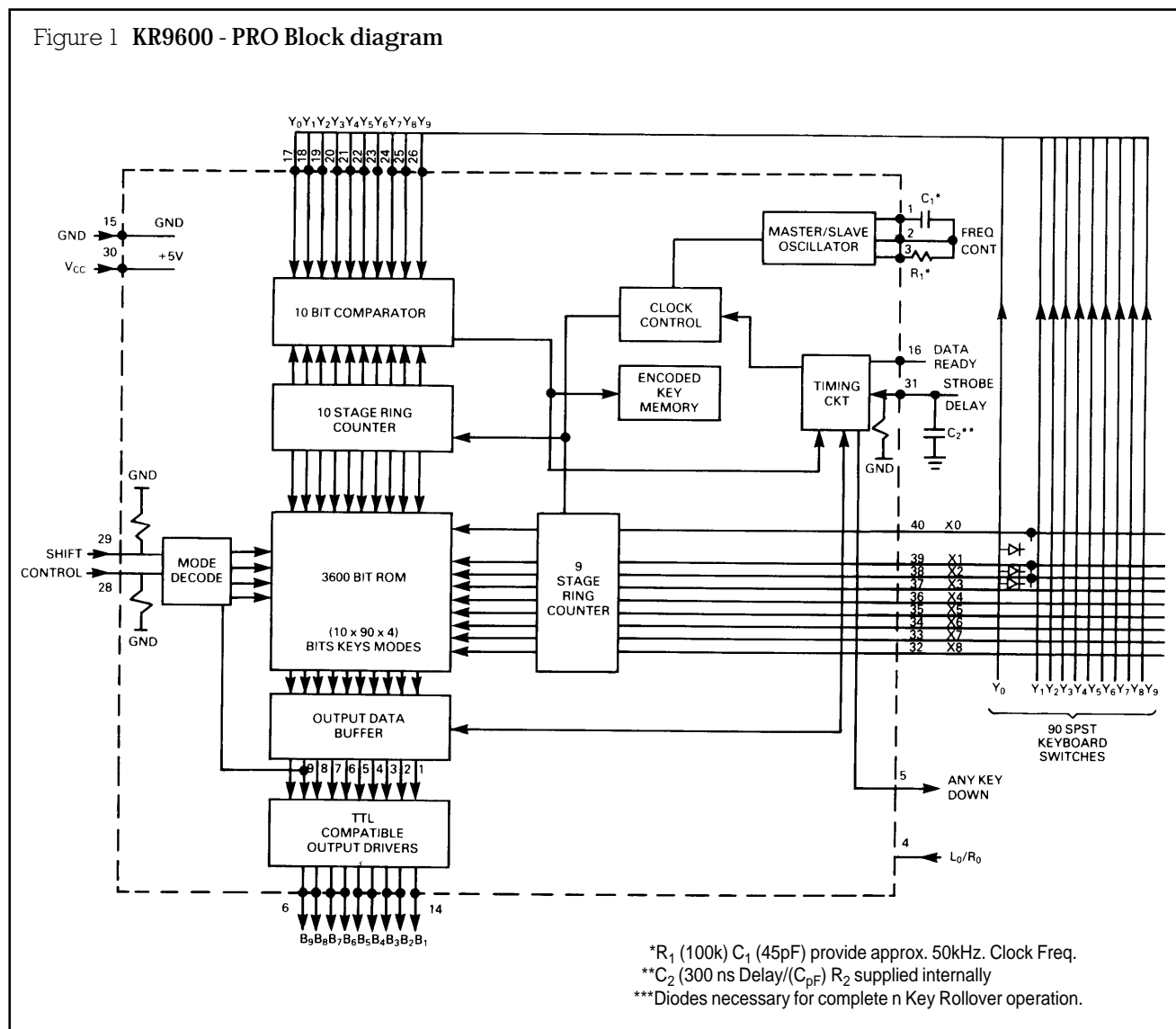
- On-chip contact bounce elimination
- N-Key rollover or lockout operation
- TTL compatible data outputs
- Normal, shift, control and shift-control modes
- Simple binary code output for user conversion
- Single + 5V supply.



Electrical characteristics TA = 0°C to 70°C, V_{CC} = 5V ±5%

Parameter	Conditions	Min.	Typ.	Max.	Units
dc characteristics					
Low level input voltage	Except Y inputs	2.0		0.8	V
High level input voltage					V
Y input high level		2.8			V
Y input low level				0.8	V
Input leakage current	Except Y V _{IN} = 5V			10.0	μA
Input with pull down R	V _{IN} = 5V	75		220	μA
Y inputs	V _{YIL} = 1V	-100	-400	-500	μA
Output voltage levels					
Low level	I _{OL} = 1.6mA	2.4		0.4	V
High level	I _{OH} = 100μA				V
X output voltage					V
Low level	600μA clock high		0.4		V
High level	I _{OH} = 10μA	2.0	4.0		V
Input capacitance	All inputs			10	pF
Power supply current			20	40	mA
ac characteristics					
Clock frequency		0.01		0.1	MHz
Chip enable access time				250	ns
Switch characteristics					
Contact resistance				300	Ω
closed					Ω
open		10			MΩ

Figure 1 KR9600 - PRO Block diagram



Operation

The keys are scanned in a nine output by ten input matrix, each key having a unique input-output combination connected to it. The inputs all go selectively to a level detector which has logically variable (1's and 0's) levels and hysteresis. The outputs are enabled one at a time from output X0 towards X8, at a rate of 10-100kHz, through a 9 stage counter. The 10 inputs are searched one at a time from Y0 to Y9, through a 10 stage ring counter, each time one of the outputs is enabled. The output and input pins all have pullups to V_{cc} and are precharged each clock even if the scan is stopped at one key. When a level on the selected path to the comparator matches a level on the corresponding comparator input from the 10 stage ring counter and the key has not been encoded, the switch bounce delay network is enabled. The key down stroke is examined without advance to the next key location, until the key has been stable for the length of the DELAY CAP pin to discharge. The code for the depressed key is transferred to the output data buffer and the data ready signal appears.

The scan has two modes as determined by the L0ckout/Rollover option. Once a key is determined to be down the scan will not advance if in the L0ckout mode. Consequently a new key closure is not detected until the previously depressed key is released. The scan sequence will resume upon key release and the output data buffer stores the code of the last key encoded. In the Rollover mode a "1" is stored in the encoded key memory and the scan sequence is resumed and the code for the last encoded key remains in the data output buffer. Each depressed key is encoded regardless of the state of the previously depressed keys. The internal keyboard ROM is 10 bits wide. Bits 1-8 are output via outputs B1-B8.

Description of pin functions

Name	Symbol	Pin	Function
X outputs	X0-X8	40-32	External outputs from the 9-stage ring counter to the keyboard to form X-Y matrix with the keyboard switches as the crosspoints.
Y inputs	Y0-Y9	17-26	External inputs from the keyboard X-Y matrix
Clock		CK	1-3 Oscillator connection pins
Any key down	AKO	5	Output indicator of key closure
Data outputs	B9-B1	6-14	Data outputs B1-B9 parallel outputs
Data ready	DR	16	This output is a pulse which signals that a key closure has been detected and that data is available at the output port.
Delay node input	Delay	31	Externally controllable delay network for eliminating the effect of switch contact bounce.
Shift input	Shift	29	This input is used to select the shift mode data
Control input	CNTRL	28	This input is used to select the control mode data. Simultaneous assertion of shift and control inputs will place the encoder into the shift-control mode.
Lockout/rollover	LO/RO	4	Selects the mode of operation for key scan
Power supply	V_{cc}	30	+5V power supply
Ground	Gnd	15	Ground

Oscillator:

The main clocks are derived from the Internal oscillator, three pins (pins #1,2,3) for frequency selection via an external resistor and capacitor are used.

Lockout/Rollover: LO/RO

This option selects the operation of the key scan when a new key is detected. In Lockout the scan stops as long as the key is down. In Rollover the scan stops till the new key is debounced by the DELAY CAP and the key code is output. Then the key position is marked as down and the scan continues until another new key is seen. The option is selected by an external pin. Lockout is active high and an on chip pulldown resistor is included.

Data ready:

The data ready pin gives a pulse upon an output state ready to transfer. This transfer occurs when a new key is encoded or when the current key is repeated.

Any key down: AKO output

The AKO output is an indicator to tell there is at least one key determined to be depressed. The output is logic high (true).

Shift control: SC

These two pins determine the output in response to a new key being detected. See coding sheet for specific outputs.

Minimum switch closure

$$T = \text{Switch bounce} + (90 \times 1/f) + \text{Strobe delay} + \text{Strobe width}$$

|
|
|
|

maximum
determined
determined
minimum time

expected
by frequency
by external
required by

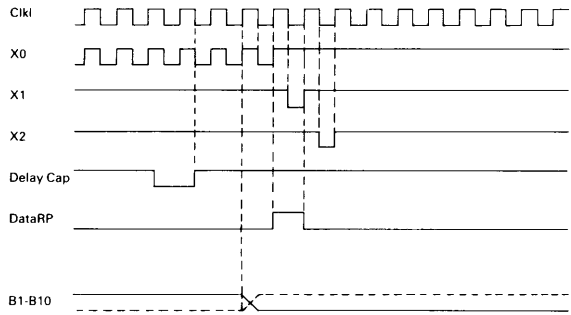
of operation
capacitance
external

circuitry

Figure 3 Timing diagram

CONDITIONS:

A key is pressed down at X0Y0 but the delay cap has not time out.
 Data Ready is high true and we have already had another key.
 DataRP = Data Ready as a Pulse.



The output of the 9600 PRO is a simple binary code which may be converted to a standard information code by a PROM or directly by a microprocessor. This permits a user maximum flexibility of key layout with simple field programming.

The code in the 9600 is shown in Table 1. The format is simple: output bits, 9,8,7,6,5,4 and 1 are a binary sequence. The count starts at X0, Y0 and increments through X0Y1, X0Y2...X8Y9; bit 9 is the LSB; bit 1 is the MSB.

Bit 2 and 3 indicate the mode as follows:

Bit 2	Bit 3	Mode
0	0	Normal
0	1	Shift
1	0	Control
1	1	Shift Control

For maximum ease of use and flexibility, an internal scanning oscillator is used, with pin selection of N-key lockout (also known as 2-key rollover) and N-key rollover. An 'any-key-down' output is provided for such uses as repeat oscillator keying.

Figure 2 Oscillator and strobe selection graphs

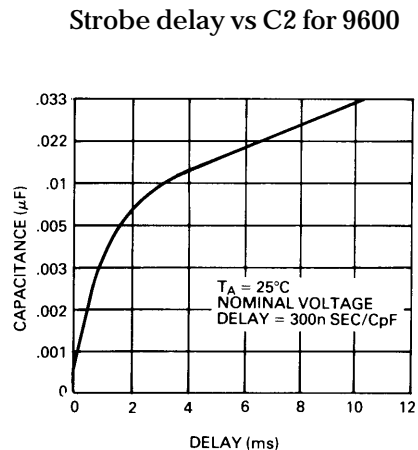
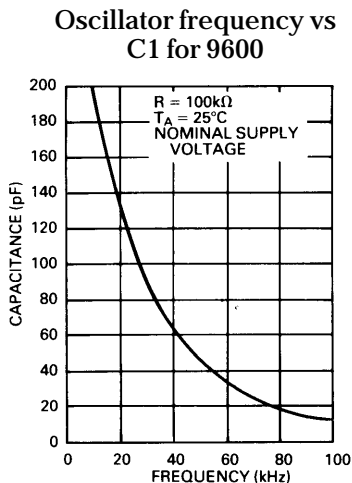


Table 1 9600-Pro coding sheet

XY	Normal B-12345678910	Shift B-12345678910	Control B-12345678910	Shift/Control B-12345678910
00	00000000	00100000	01000000	01100000
01	00000001	00100001	01000001	01100001
02	00000010	00100010	01000010	01100010
03	00000011	00100011	01000011	01100011
04	00000100	00100010	01000100	01100100
05	00000101	00100011	01000101	01100101
06	00000110	00100011	01000110	01100110
07	00000111	00100011	01000111	01100111
08	00001000	00100100	01000100	01100100
09	00001001	00100101	01000101	01100101
10	00001010	00100101	01000110	01100110
11	00001011	00100101	01000111	01100111
12	00001100	00100110	01000110	01100110
13	00001101	00100110	01000111	01100111
14	00001110	00100111	01000111	01100111
15	00001111	00100111	01000111	01100111
16	00010000	00101000	01001000	01101000
17	00010001	00101000	01001001	01101001
18	00010010	00101001	01001010	01101010
19	00010011	00101001	01001011	01101011
20	00010100	00101010	01001010	01101010
21	00010101	00101010	01001011	01101011
22	00010110	00101011	01001011	01101011
23	00010111	00101011	01001011	01101011
24	00011000	00101000	01001000	01101000
25	00011001	00101001	01001001	01101001
26	00011010	00101010	01001010	01101010
27	00011011	00101011	01001011	01101011
28	00011100	00101100	01001100	01101100
29	00011101	00101101	01001101	01101101
30	00011110	00101110	01001110	01101110
31	00011111	00101111	01010000	01110000
32	00100000	00110000	01010000	01110000
33	00100001	00110001	01010001	01110001
34	00100010	00110001	01010010	01110010
35	00100011	00110001	01010011	01110011
36	00100100	00110010	01010010	01110010
37	00100101	00110010	01010011	01110011
38	00100110	00110011	01010011	01110011
39	00100111	00110011	01010011	01110011
40	00101000	00110100	01010100	01110100
41	00101001	00110100	01010101	01110101
42	00101010	00110101	01010101	01110101
43	00101011	00110101	01010101	01110101
44	00101100	00110101	01010100	01110100
45	00101101	00110101	01010101	01110101
46	00101110	00110110	01010110	01110110
47	00101111	00110111	01010111	01110111
48	00110000	00111000	01011000	01111000
49	00110001	00111000	01011001	01111001
50	00110010	00111001	01011001	01111001
51	00110011	00111001	01011001	01111001
52	00110100	00111010	01011010	01111010
53	00110101	00111010	01011010	01111010
54	00110110	00111010	01011010	01111010
55	00110111	00111011	01011011	01111011
56	00111000	00111100	01011100	01111100
57	00111001	00111100	01011101	01111101
58	00111010	00111101	01011101	01111101
59	00111011	00111101	01011101	01111101
60	00111100	00111100	01011100	01111100
61	00111101	00111101	01011101	01111101
62	00111110	00111110	01011110	01111110
63	00111111	00111111	01011111	01111111
64	10000000	10100000	11000000	11100000
65	10000001	10100001	11000001	11100001
66	10000010	10100001	11000010	11100010
67	10000011	10100001	11000011	11100011
68	10000100	10100010	11000010	11100010
69	10000101	10100010	11000011	11100011
70	10000110	10100011	11000011	11100011
71	10000111	10100011	11000011	11100011
72	10000100	10100100	11000100	11100100
73	10000101	10100101	11000101	11100101
74	10000101	10100101	11000101	11100101
75	10000101	10100101	11000101	11100101
76	10000110	10100100	11000100	11100100
77	10000110	10100101	11000101	11100101
78	10000110	10100110	11000110	11100110
79	10000111	10100111	11000111	11100111
80	10001000	10101000	11001000	11101000
81	10001001	10101001	11001001	11101001
82	10001010	10101001	11001010	11101010
83	10001011	10101001	11001011	11101011
84	10001010	10101010	11001010	11101010
85	10001010	10101010	11001010	11101010
86	10001011	10101011	11001011	11101011
87	10001011	10101011	11001011	11101011
88	10001100	10101100	11001100	11101100
89	10001101	10101101	11001101	11101101

Internal Oscillator (Pins 1, 2, 3)
 Lockout/Rollover (Pin 4)
 Internal Resistor to GND
 Lockout is Logic 1

Pulse Data Ready
 Any Key Down (Pin 5) Positive Output
 Internal Resistor to GND on Shift
 and Control Pins

Applications

Figure 4 shows a PROM-encoded 64 key, 4 mode application, using a 256 × 8 PROM, and Figure 5 a full 90 key, 4 mode application utilising a 512 × 8 PROM.

If N-key rollover operation is desired, it is recommended that a diode be inserted in series with each switch as shown. This prevents 'phantom' key closures from resulting if three or more keys are depressed simultaneously.

Figure 4 9600-PRO typical application 64 key, 4 mode

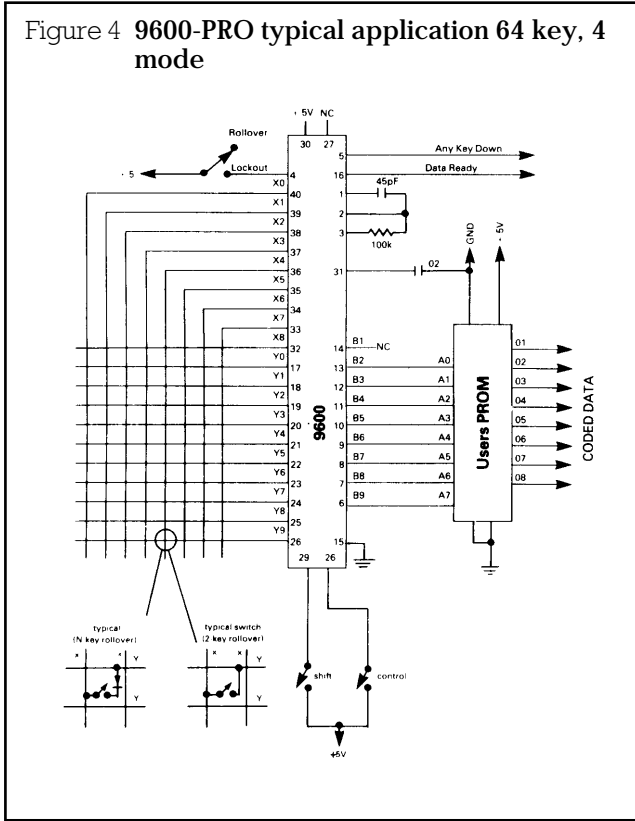
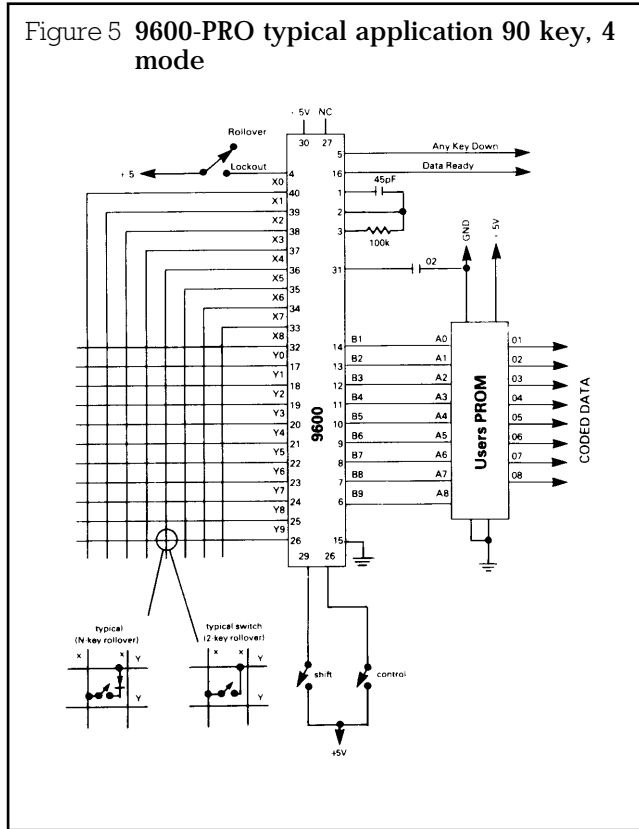


Figure 5 9600-PRO typical application 90 key, 4 mode



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