FUNCTIONAL DESCRIPTION OF THE PROFILE ANALOG BOARD

(Refer to the six page schematic for reference details)

The following document has been written with the purpose of describing the circuitry on the Profile Analog Board in detail. It is not meant to be a troubleshooting guide, but is aimed at informing the technician of the different circuits and operating parameters of the board. This document should be used with the Profile Analog Board Tester, Apple Part # 890-0184, in testing and repairing any problem on the board.

In the event that it is desired to troubleshoot the board onboard the Profile unit itself, the board may be accessed using the following method:

Turn the Profile off and let it sit for a minute until the drive stops rotating. Access the Profile Analog board by turning the Profile over on its top, providing the top cover is on the unit. Remove the metal cover under the cabinet which accesses the Analog board. Power the drive back up and refer to the schematic for the test points and waveforms. No harm can come to the drive while it is running in this position, but random data errors will probably occur. Make sure that the drive cannot fall over or receive any sharp jolt or shock as this will damage the HDA media.

223 direct.

0+1 - Spare or 0+1

The connector J2 on the left connects the Analog board to the Controller board. The signals coming into the board are the write data (NRZWDTA), the 10mhz write clock (2F), the write precompensation and current control signal (PCOMP-LOCUR), and the write gate signal (WTGT). Outputs to the Controller board are the TRK 0 detection and Index pulse signals coming from the HDA assembly. Power and ground inputs to the board are also shown for reference.

The track 0 signal indicates when the head stepper motor assembly is at track 0 or the outer track location, while the index pulse occurs once per drive revolution. The index pulse can be monitored at test point TP-9 and used as an oscilloscope trigger for viewing the track analog data at test point TP-1.

The +/- 0A and +/- 0B stepper motor control phases pass through the board and are routed to the HDA stepper motor at connector J7.

The Track 0 signal is obtained from the photosensor mounted on the HDA stepper motor. The sensor is tripped by the rotating arm assembly on the motor shaft when the head array is at the track 0 position, and the sensor output comes in the board at connector J6. The signal is detected and amplified by device UC30 and passed to the Controller board at J2 pin 2.

The Index signal comes from the photosensor mounted under the HDA. The sensor is tripped by a small metal tab fastened to the bottom plastic cover of the drive spin motor and comes in the board at connector J8. The signal is detected and amplified by device UC30 and passed to the Controller board at J2 pin 4.

The write encoding and precompensation circuitry consists of devices UC27, 28, 29, and 30. The 10mhz write clock is divided by UC2 to create a 5mhz clock (1F) for VCO reset control purposes. The data and control signals are decoded by the PAL logic array UC28, and DLY 2 provides delay references of 10 and 20nsec for data signal precompensation.

This is done to compensate for the magnetic fluxes on the disk media trying to repel each other because of their polarity differences. If this happens, the flux reversals on the media will all have more or less the same distance between them, resulting in a sine wave pattern on the disk with no 1F or 2F signal component margin between flux reversals.

The signal outputs of the PAL indicate Early, On Time, or Late data occurances as detected in the PAL data register. These are generated by comparing the data bit pattern and defining the three potential transition points for every flux reversal with the write timing. These signals then shift the write data signal by selecting the proper amount of delay (usually 20 nsec) to over-write any potential bit shift on the media surface. This precompensates the data on the disk surface, allowing a higher bit density without loss of resolution.

On this page are the write amplifier, write current control, head select, and read detection circuitry. The write data (WXS) is gated through UC2 into the write current driver array UC1 (MPQ6700) and UC31 (MPQ2907). The data through UC2 will be blocked if the WRTSM' write sector mark signal is true, as this is used to write blank areas on the track for disk sector formatting identification.

The current level of the final driver transistor array is set by a voltage reference developed across zener CR1. This diode has a value of 1.2 to 1.25 VDC, which sets the drive level of UC1 to 24ma of write current (48ma peak-to-peak).

This level is used to write tracks 0 through 128, while tracks 129 to 152 use less current because of the thinner media coating and smaller disk radial area per bit on the inner tracks. Remember that the drive spin is a constant speed, and the head covers more area on an outer track than it does an inner track during the same time period. In addition, the media surface coating on the disk is thinner towards the center. The smaller available area requires less current to effectively write the media than the larger.

To set the lower current value, the PCOMP-LOCUR' (Precompensation- Low Current) signal goes active, causing UC3 to "steal" 5ma from the write current value through the 1.78kohm resistor R10. This results in a lower head write current level of 19ma (38ma peak-to-peak) for the inner tracks.

The write current passes through diodes CR4 and CR13 to four connector pins ABCD, and from there directly to the heads. If desired, a pin to pin wire loop can be used at pins AB or CD to monitor the actual write current with a current probe, as the pins are shunted with 22 ohm resistors to the head matrix.

Signals HS-1 and HS-0 are decoded by 1 of 4 decoder UC4. The output selects one of the four heads for either reading or writing by correctly biasing the center tap of the head coil. The other heads are held in an off condition allowing only one head to be selected at a time.

The POWEROK signal is a monitor function of the power supply and instantly terminates any write signal if the main power to the Profile unit is lost. The POWEROK line is dropped low by the power supply if the incoming AC is lost, causing the voltage drop across R16 to turn on UC13. This cuts off UC1 while there is still power out of the supply maintaining the system electronics. The POWEROK signal also holds the stepper motor, Z8 controller, and write amplifiers off for a brief moment after initial power on. This delay action can be seen by the READY lamp on the front panel lighting for 1 to 1 & 1/2 seconds when Profile power is first turned on.

The WRTSM' signal is used to "write" (actually erase) the track sector marks. The Profile uses 16 blank sector marks per track radially aligned on the disk, and this signal inhibits any write action to the head during the formatting of the these areas on the disk.

The sector marks are erased as 20usec long blank spaces and the disk read logic needs a minimum of 10usec to identify the mark. If any sector mark on a track is written over, the data in that sector is effectively destroyed and cannot be used.

For read operation the forward biased diode matrix detects the differential analog transitions (-X and -Y) of the selected head. The other heads are biased so that there is no current flow in the coil, preventing any signal detection. The analog signal transitions are extremely small and attempting to view them in this diode network is impossible.

The -X and -Y analog signals enter the ECL 10114 preamplifiers, which are power supply isolated by RG1 for noise immunity. The 10114 was selected because of its excellent input geometry with very little noise. The signals then pass through a low pass filter which is set for 7.5Mhz, or 3 times the maximum read signal frequency of 2.5Mhz (2F).

This filter attenuates the major error element of the detected signal, which is the third harmonic of the flux reversal. If viewed on a scope, this is the "knee" part of the waveform transition midway between signal peaks. The signal then enters a 592 video amplifier UC6, which acts as the AGC (Automatic Gain Control) integrator and controller.

The AGC level is developed by device Q3, a VCR2N junction whose bias level is controlled by UC8, a 353 AGC detector and amplifier. The AGC controlled output of the 592 passes through an emitter follower and buffer network UC7 and is available for monitoring purposes at test points TP1 and TP2 at the bottom of the page. These are differential signals and can be shown individually or compared with each other.

The signal levels at these test points are still analog in form and should be around 1.5 to 2 volts peak-to-peak. Anything outside of these levels is indicative of a bad AGC network and renders the data unreadable to the system. If the AGC is lost, the Profile cannot perform the initial scan function after power up.

If this should happen, suspect anything in this network. However, remember that the signals into the circuit are far too small to be monitored directly. The best way to troubleshoot anything in this area is to swap out the ICs in the circuit. Troubleshooting to a bad component other than an IC is almost impossible and the board may have to be scrapped out if any other component is at fault.

To the right of the UC8 pin 7 is a jumper used to set the AGC at a fixed level referenced to -12VDC. This is done only in board manufacture test and the jumper should never be found in the field. Remove it if installed.

The AGC controlled analog signals enter two 10116 ECL schmitt level circuits (UC9) which make up the zero crossing detector. If any signal dropout occurs because of poor AGC, it will be detected by this circuit and interpreted as data.

The upper portion of the circuit sets the gain for a minimum amplitude symmetrical signal level. The lower circuit has a delay line in parallel which acts as a 1/4 wavelength delay line through the sum and cancel effect on the signal. In addition, the delay line acts as a good low pass filter to eliminate "hash". The output of the OR gate UC10 is the detected signal pulse. This is allowed to happen only during the "signal allowed" period set by the delay circuit.

The detected signal is then gated through UC11 which outputs a low going pulse for every signal that is detected by the zero crossing detector circuit. The output of UC11 is developed by an RC network consisting of C20, R65, and R66, which forms a 50nsec pulse for every flip-flop transition of UC11. If the pulse width is less than 40nsec, capacitor C20 should be replaced to increase the time factor and corresponding pulse width.

As previously outlined, Profile uses blank areas on the track for sector identification. These marks indicate the 16 individual track sectors and are placed on the track when it is initially formatted. If any sector mark is over-written or lost, that one sector cannot be read by the system and the data within it is lost.

Another schmitt trigger device (UC13) coupled with a slow response time RC circuit is used to detect these blank marks and will not detect any "no signal" period less than 10usec long. The input develops the signal across CR18, CR19, and CR20 with the RC circuit of C23 and R74 delaying the response of one side of UC13.

This means that sector cannot be detected if any noise or off track data has overwritten the blank disk area to the point where it is less than 10usec long. The sectors are written in 20usec period during formatting, so some degradation can occur before the sector is completely lost.

The AM HOLD or address mark hold is a function of the Write Sector Mark and Write Gate signals on page 2. It is used to clamp the circuit during write operations, which prevents the output from indexing any data to the controller card.

On this page are the VCO (Voltage Controlled Oscillator) phase comparator control and data output circuits.

The read gate RDGT provides the control element for the circuit. The VCO is reset during any "no read" condition by the 1F 5Mhz signal. This allows the VCO to be triggered almost instantaneously by the RDGT signal instead of recovering from an extreme compliance condition. The circuit at the top of the page sets the time constant of the reset signal (usually a few microseconds).

When the read gate goes active it triggers the VCO. The circuit then acts to lock the leading edge of the VCO pulse to the leading edge of the 50nsec signal data pulse. This is done by phase comparing the data pulse with the VCO pulse and generating a corresponding +/- INC or +/- DEC control signal. This pulse goes to the charge pump on page 6 which controls the VCO operating frequency. It takes about 20 read data pulses to properly control the VCO as the pulse train consists data pulses at different intervals due to MFM criteria.

The net effect of the VCO control is to compensate for any difference between the read circuit timing and the speed of the disk. Any speed difference creates an error in the data decoding as the data has to occur at 200nsec cycle periods. The VCO compensates for this, allowing a motor speed deviation of up to 3%.

The circuit does this by acting as a "lock", which keeps the data referenced to the center of the VCO pulse "window". The lock lines up the data pulse in the center of the window for stability and proper detection. The VCO output and the data pulse can be monitored at (TP6 and TP7, respectively) to verify the leading edge of both signals occurring simultaneously.

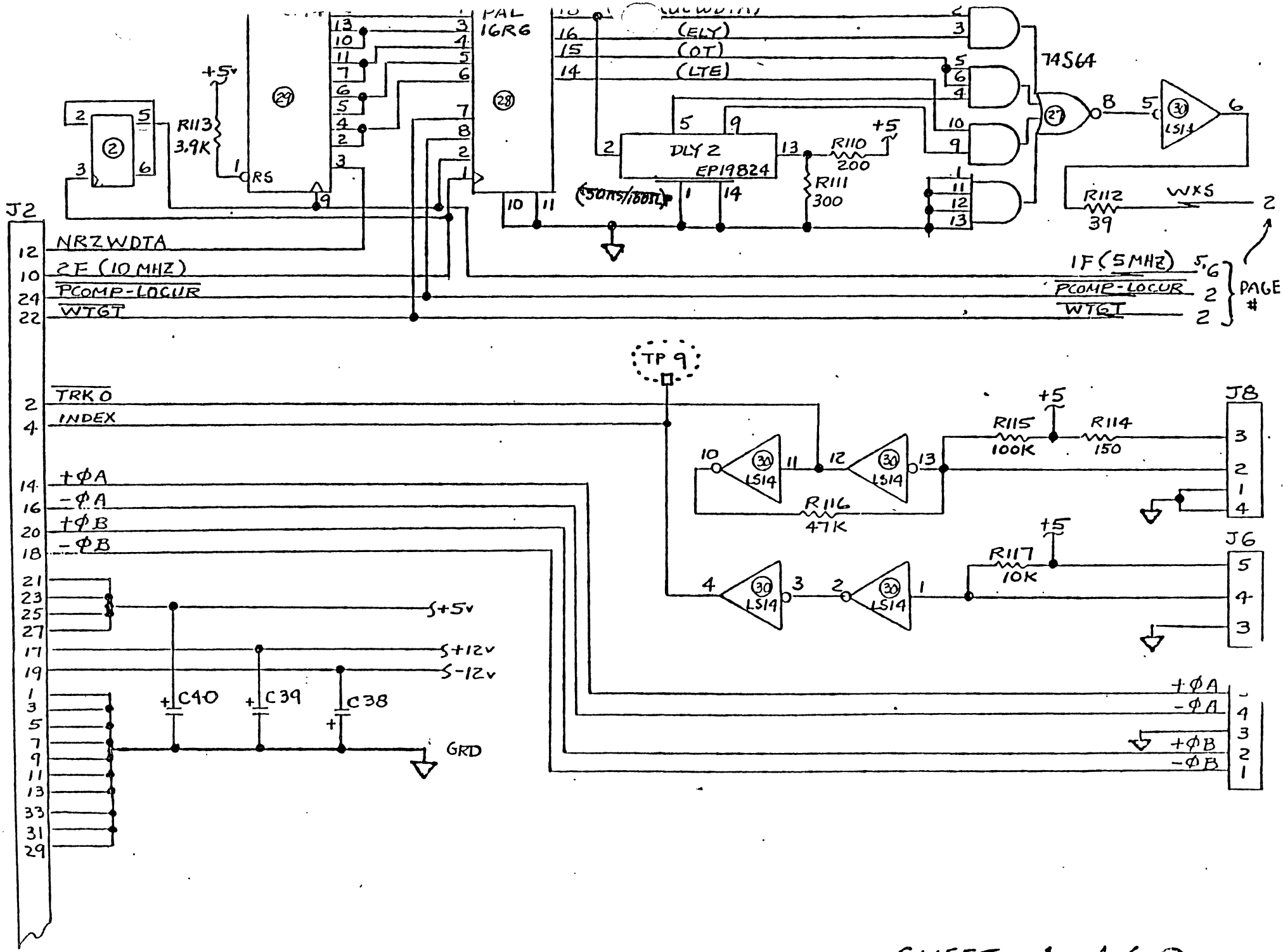
The last portion of the circuit is the ECL to TTL level transition network at the bottom of the page. The detected NRZ data and clock signals are fed to the Controller board through connector J2.

PAGE SIX

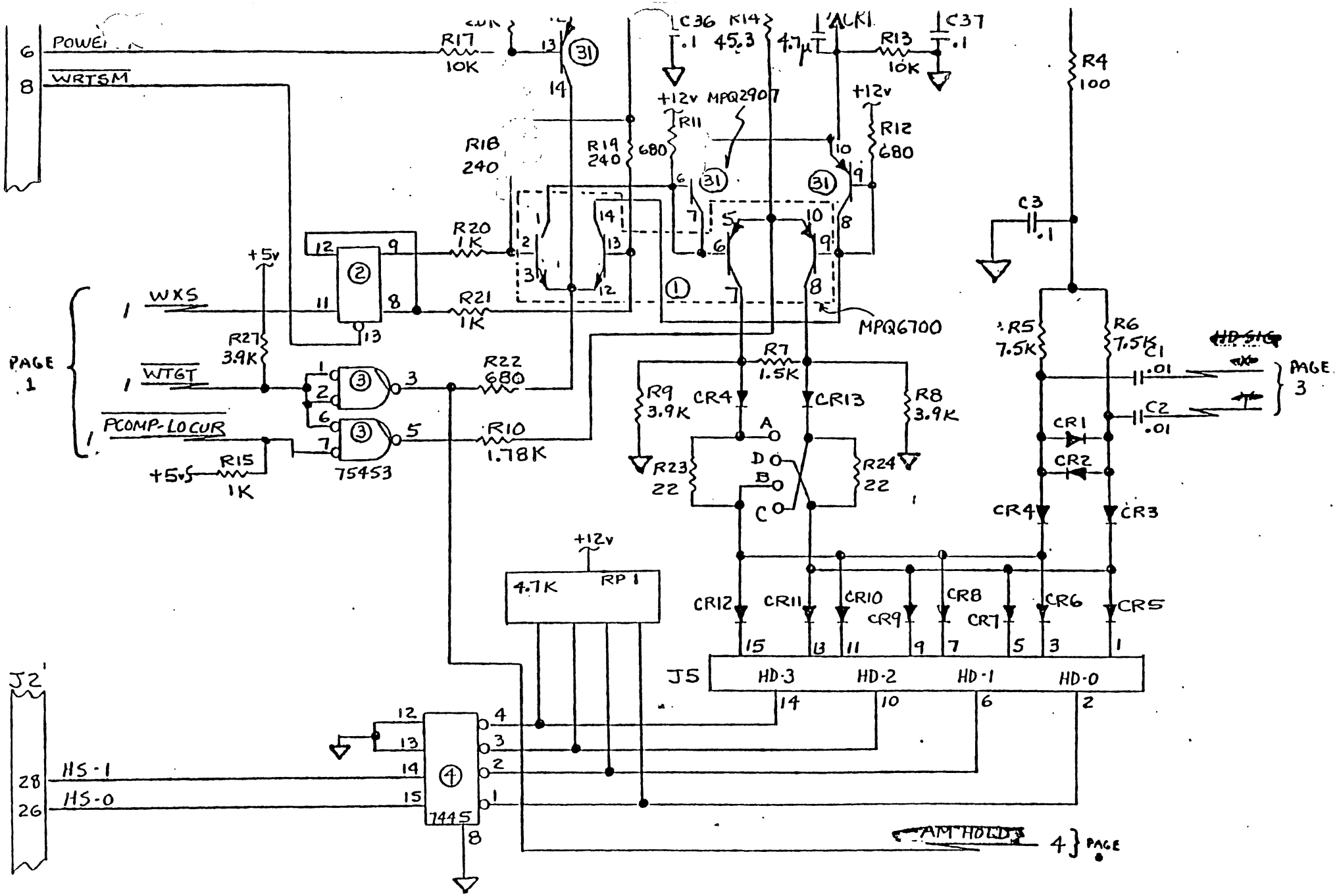
On this page is the VCO circuit itself. The main portion of the circuit is the "charge pump" formed with UC24 and the network around it. The voltage level of the circuit is controlled by the INC -/+ and DEC -/+ signals from page 5. The input of the network acts as a "sample and hold" circuit, setting the current level of the ouput transistors.

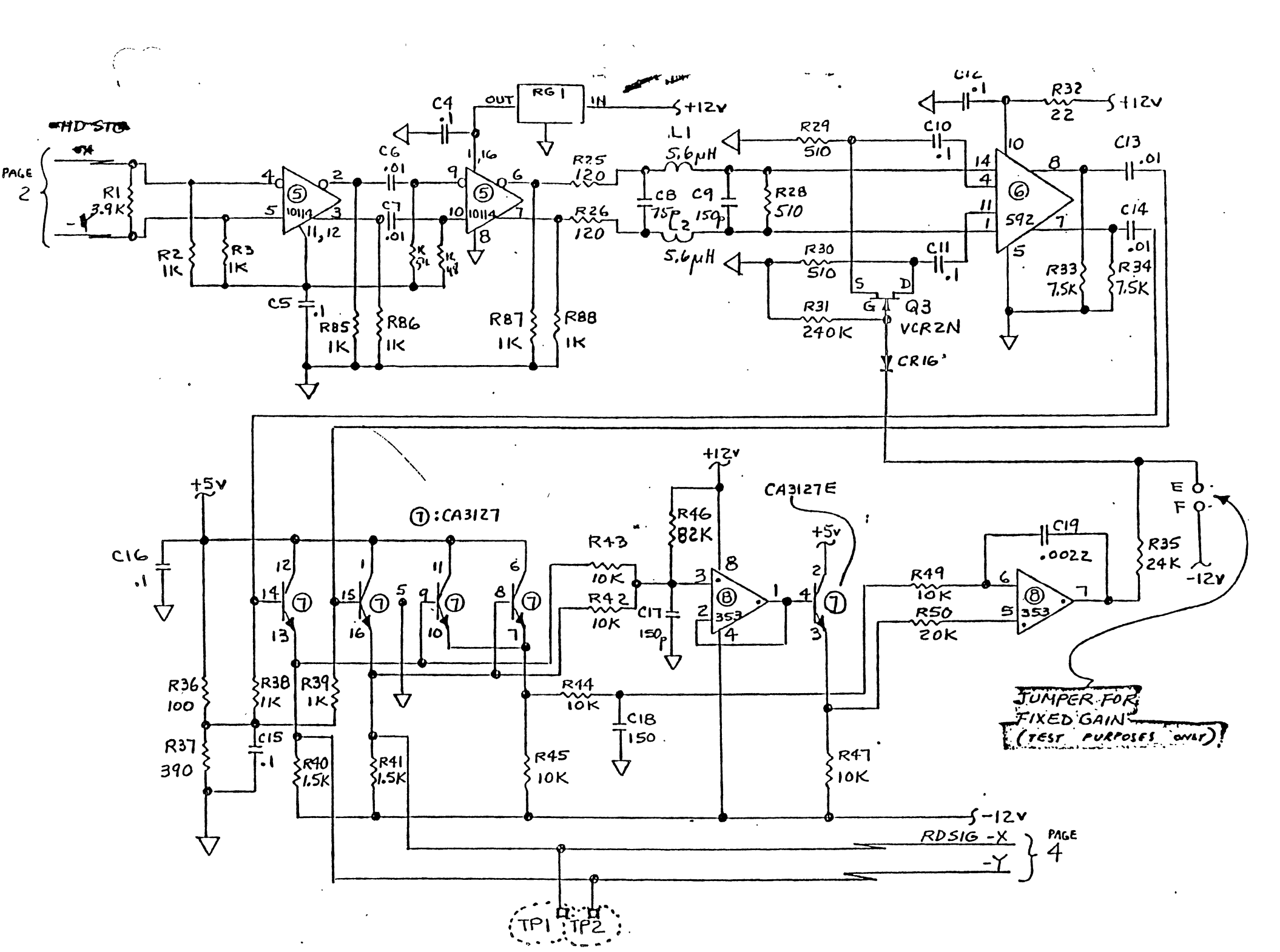
The output passes through a low pass RC filter to a buffer amp UC25. This serves to buffer the current that sets the voltage control level at the MV104 varactor, controlling the VCO frequency. The output of the charge pump can be monitored at TP8.

The VCO output is approximately 20Mhz, and is routed to UC22 on page 5. This is a divide by 4 circuit and the resulting 5Mhz signal is the 200nsec VCO "window" into which the incoming read data is locked.

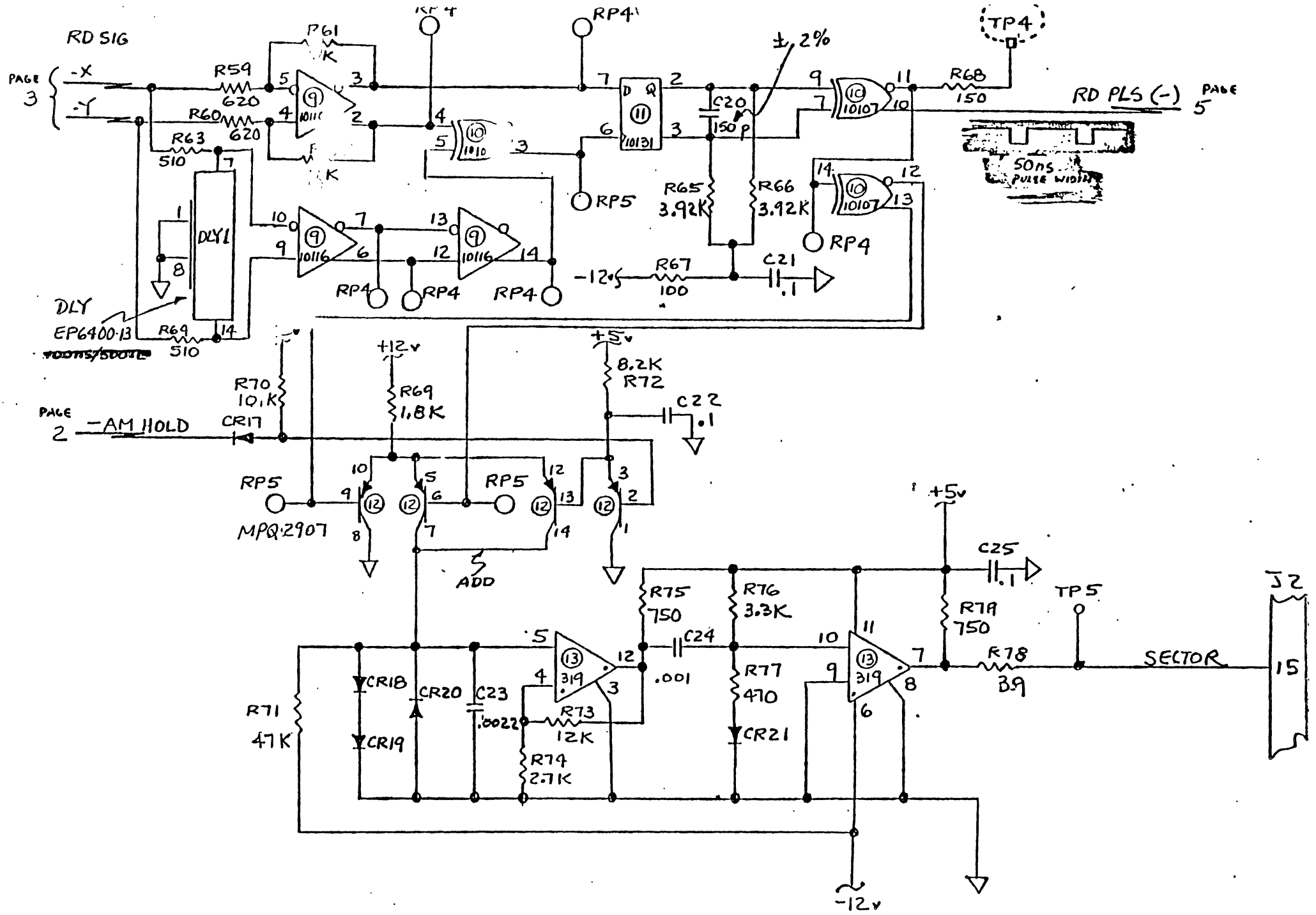

PAL 16R6
(ELY)
(OT)
(LTE)
74S64
DLY 2
EP19824
(50ns/180ns)
R110 200
R111 300
R112 39
WXS
R113 3.9K
RS
+5
J2
NRZWDTA
2F (10 MHZ)
PCOMP-LOCUR
WTGT
IF (5MHZ)
PCOMP-LOCUR
WTGT
PAGE #
TP 9
TRK 0
INDEX
+ΦA
-ΦA
+ΦB
-ΦB
LS14
R115 100K
R114 150
R116 47K
R117 10K
J8
J6
+5V
+12V
-12V
C40
C39
C38
GRD

SHEET 1 1 0

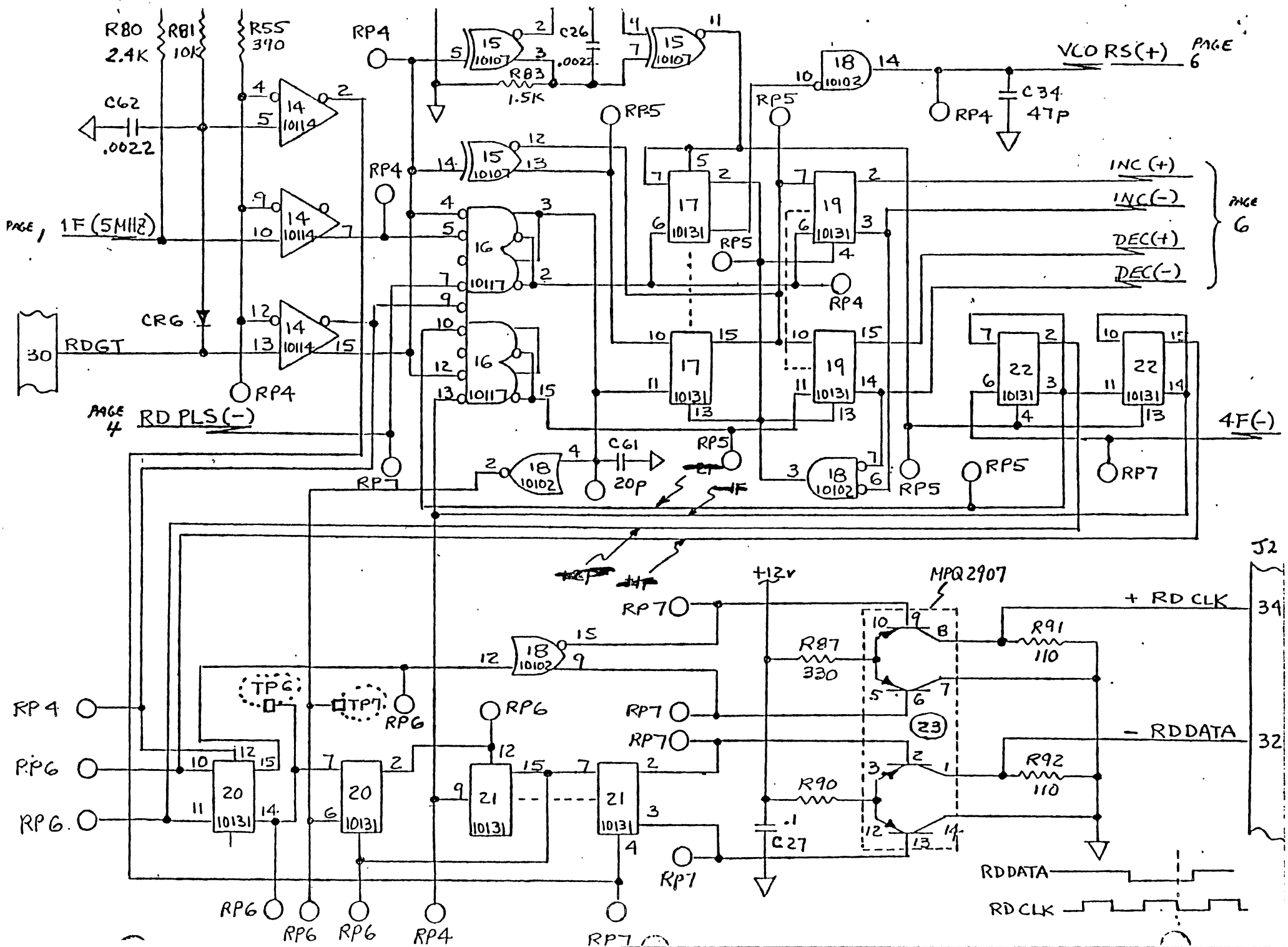

POWER
WRTSM
R17 10K
C36 .1
R14 45.3
4.7µ
ALK
C37 .1
R13 10K
R4 100
+12v
MPQ2907
R11 680
R12 680
R18 240
R19 240
C3 .1
R20 1K
R21 1K
+5v
WXS
WTGT
PCOMP-LOCUR
R27 3.9K
R22 680
R10 1.78K
R15 1K
+5v
75453
MPQ6700
R7 1.5K
R9 3.9K
R8 3.9K
CR4
CR13
R23 22
R24 22
R5 7.5K
R6 7.5K
C1 .01
C2 .01
CR1
CR2
CR4
CR3
PAGE 1
PAGE 3
+12v
4.7K
RP 1
CR12
CR11
CR10
CR9
CR8
CR7
CR6
CR5
J5
HD-3
HD-2
HD-1
HD-0
J2
HS-1
HS-0
7445
AM HOLD
PAGE 4

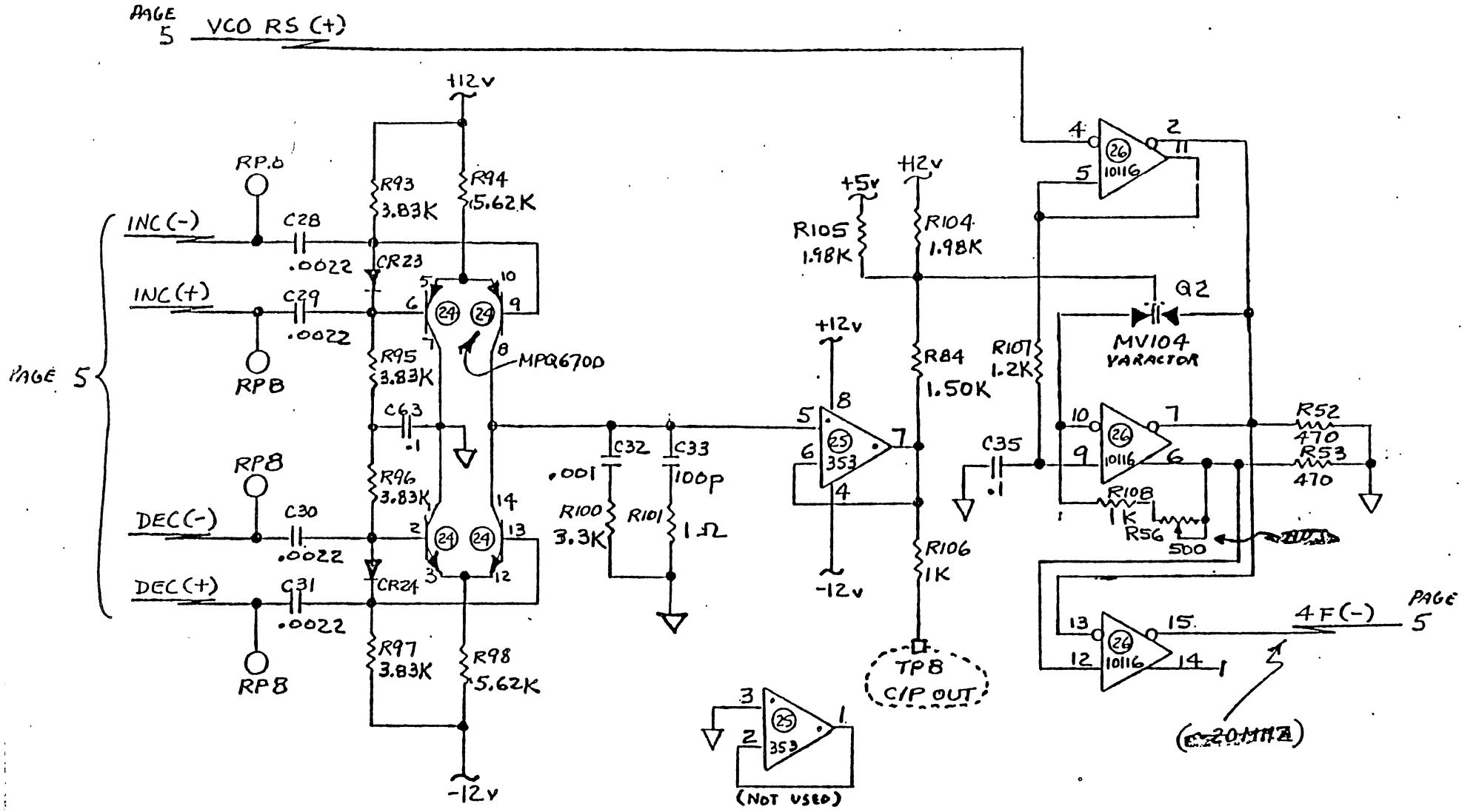

HD STD
PAGE 2
R1 3.9K
R2 1K
R3 1K
C4 .1
RG1
OUT
IN
+12V
C6 .01
C7 .01
C5 .1
R85 1K
R86 1K
R87 1K
R88 1K
R25 120
R26 120
L1 5.6µH
L2 5.6µH
C8 75p
C9 150p
R28 510
R29 510
R30 510
R31 240K
C10 .1
C11 .1
C12 .1
R32 22
C13 .01
C14 .01
R33 7.5K
R34 7.5K
Q3 VCR2N
CR16
⑦:CA3127
CA3127E
+5V
C16 .1
R36 100
R37 390
R38 1K
R39 1K
C15 .1
R40 1.5K
R41 1.5K
R42 10K
R43 10K
R44 10K
R45 10K
R46 82K
C17 150p
C18 150
R47 10K
R49 10K
R50 20K
C19 .0022
R35 24K
E
F
-12V
JUMPER FOR FIXED GAIN (TEST PURPOSES ONLY)
RDSIG -X
-Y
PAGE 4
TP1
TP2

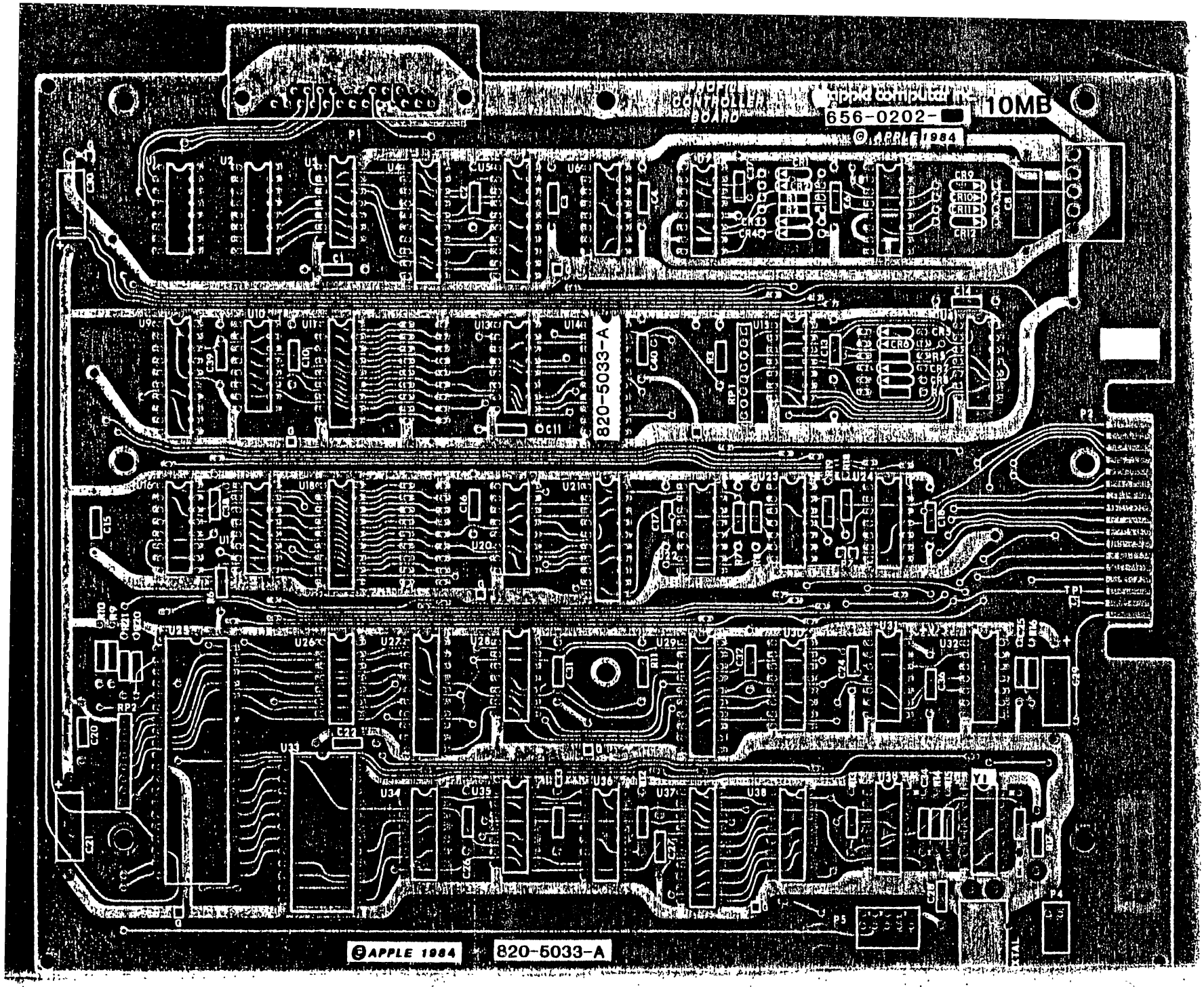
SHEET 7 OF 6


RD SIG
PAGE 3
-X
-Y
R59 620
R60 620
R61 K
K
R63 510
R64 510
DLY
EP6400-13
100NS/500NS
DLY1
10116
10111
10110
10131
10107
RP4
RP5
R65 3.92K
R66 3.92K
R67 100
C20 150 P
C21 .1
±2%
R68 150
TP4
RD PLS (-)
PAGE 5
50ns PULSE WIDTH
-12v
+12v
+5v
R69 1.8K
R70 10.1K
R72 8.2K
C22 .1
PAGE 2
-AM HOLD
CR17
RP5
MPQ-2907
ADD
R75 750
R76 3.3K
R77 470
R78 39
R79 750
C24 .001
C25 .1
TP5
J2
SECTOR
15
CR18
CR19
CR20
CR21
C23 .0022
R71 47K
R73 12K
R74 2.7K
319

SHEET 4 of 6


R80 2.4K
R81 10K
R55 390
C62 .0022
C26 .0022
R83 1.5K
RP4
RP5
RP6
RP7
VCO RS(+) PAGE 6
C34 47P
INC (+)
INC(-)
DEC(+)
DEC(-)
PAGE 6
PAGE 1 1F (5M112)
CR6
30 RDGT
PAGE 4 RD PLS(-)
C61 20P
4F(-)
+12V
MPQ2907
R87 330
R91 110
R92 110
R90
C27 .1
+ RD CLK
- RDDATA
J2
34
32
RDDATA
RD CLK
TP6
TP7


PAGE 5 VCO RS (+)
+12V
RP.6
R93 3.83K
R94 5.62K
INC (-)
C28 .0022
CR23
INC (+)
C29 .0022
RP8
R95 3.83K
MPQ6700
PAGE 5
C63 .1
RP8
R96 3.83K
DEC (-)
C30 .0022
DEC (+)
C31 .0022
CR24
RP8
R97 3.83K
R98 5.62K
-12V
C32 .001
C33 100P
R100 3.3K
R101 1Ω
+5V
+12V
R105 1.98K
R104 1.98K
+12V
R84 1.50K
R106 1K
-12V
TP8 C/P OUT
(NOT USED)
R107 1.2K
Q2
MV104 VARACTOR
C35 .1
R108 1K
R56 500
R52 470
R53 470
4F (-)
PAGE 5
(~20MA)
REV DATE: 5/5/81
DPJ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©APPLE 1984
820-5033-A
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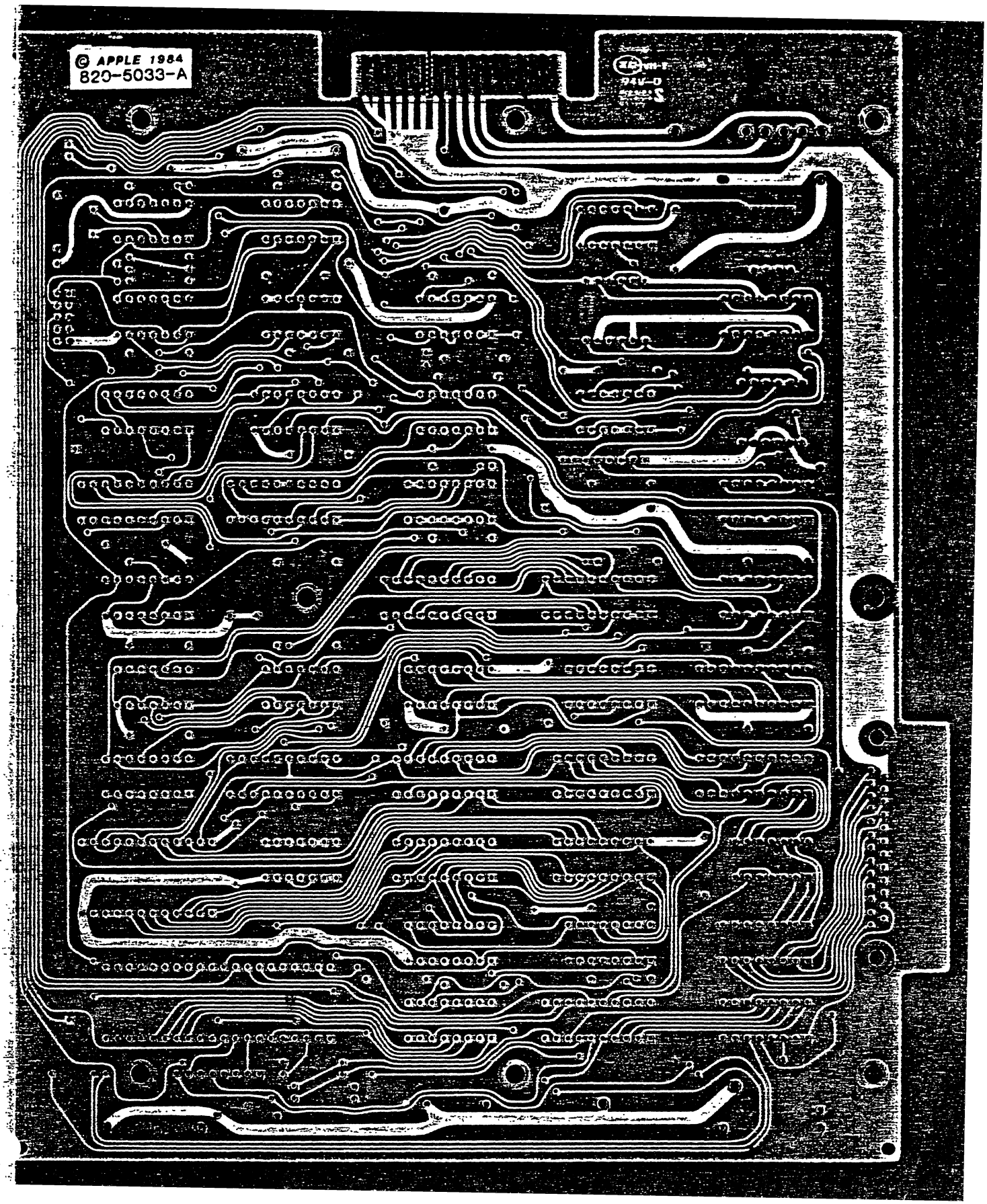
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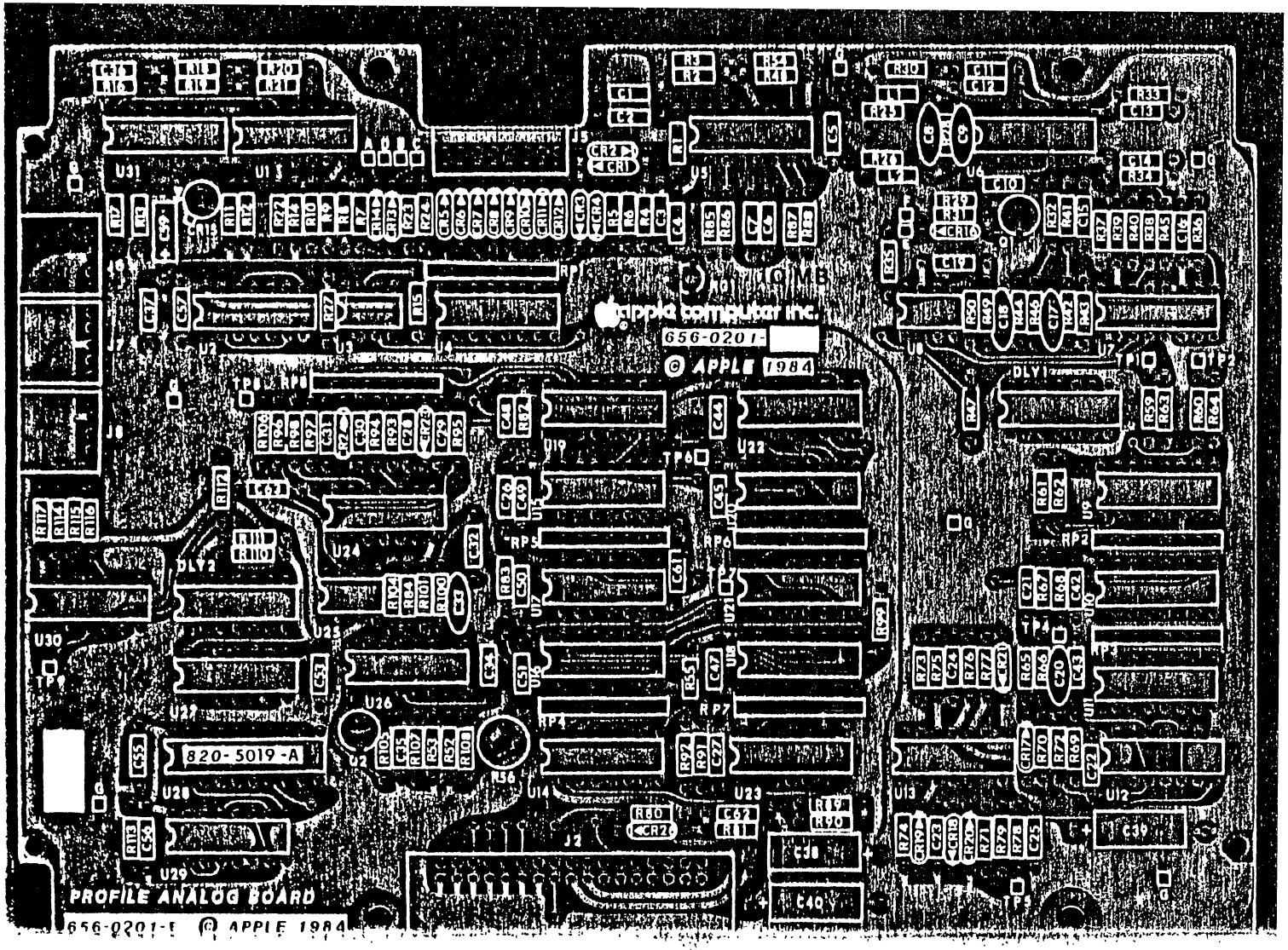
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apple computer inc.
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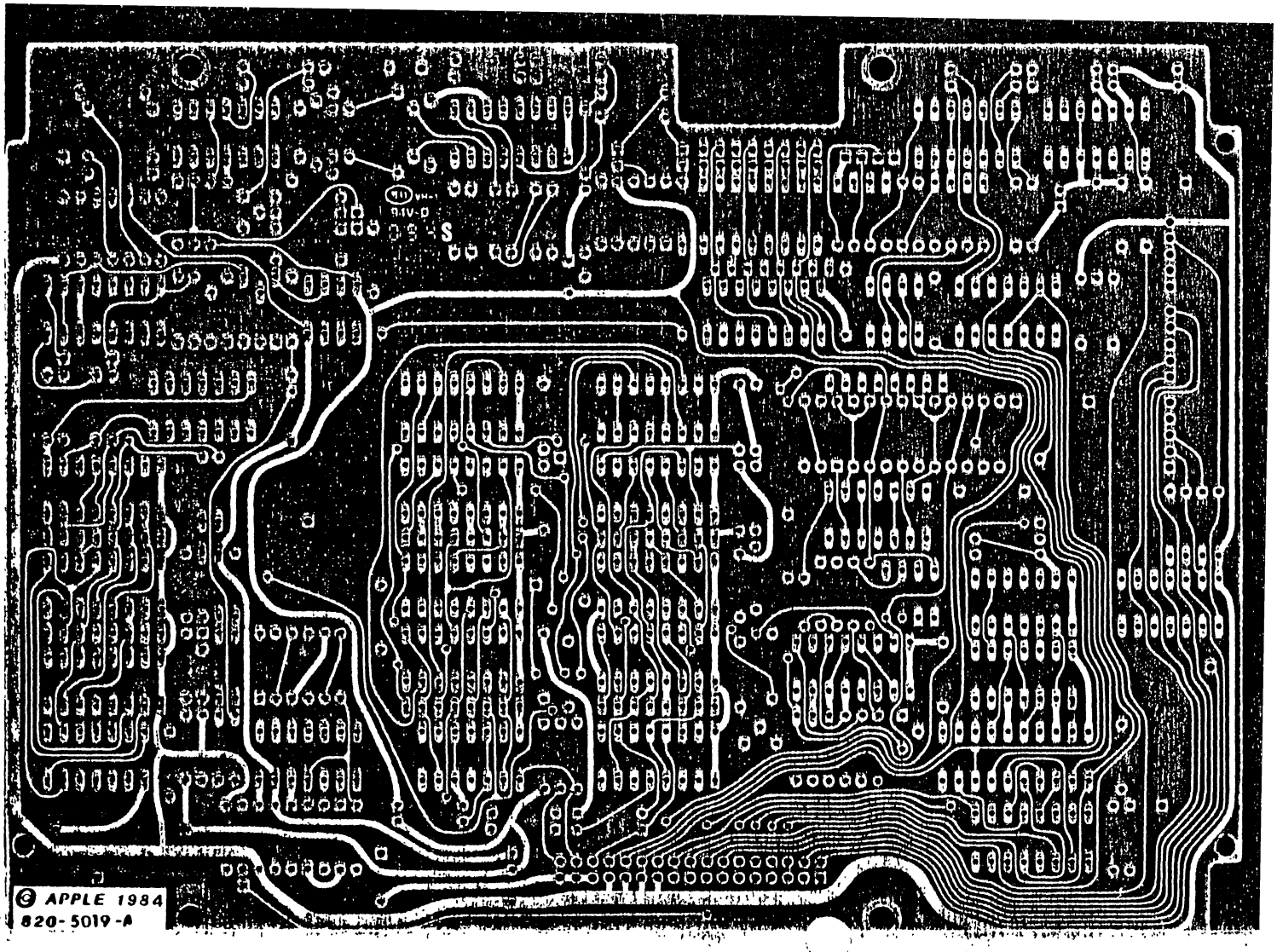
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