1984 AppleBus File Server

This brief report addresses yet another version of the file server. Characteristics of this version include:

- o 68000 based
- o AppleBus based using SCC
- o 128K RAM upgradable to 512K with 256K parts (no wait states)
- o Internal Widget Hard Disk
- o Time-of-Day Clock
- o External Parallel Port for Hard Disk (?)

The Processor

An 8MHz Motorola 68000 is used as the processor.

Memory

The file server will contain 128K bytes of RAM. This will be done by using 16 64K DRAM chips. An upgrade path for 1/2 Megabytes could will be provided for with the use of 256K DRAM parts. The 68000 is initially controlled by two ROMS, at this point the ROMS can be anywhere from 16K bits to 256K bits -- the initial configuration will probably be for two 128K bit ROMS for a total of 32K bytes of code.

Upon power-up, the ROM will appear at both address 0 and 400000 (the same as MAC). RAM appears at 800000. This initial addressing mode is called "start-up" mode. Start-up mode call only be entered by a power-on reset, or by the reset button, if one is installed.

When start-up mode is disabled, RAM appears at address 0 and ROM appears at address 400000 (the same as MAC). Start-up mode is disabled automatically by the Atlas hardware when an address in the 400000 ROM address space is accessed. Note that if the start-up address vector stored in location 0 of the ROM is within the 400000 ROM address space the Atlas hardware switches RAM to location 0 after the initial PC and stack pointers are fetched from

the ROM, thus the ROM code does not need to execute any instruction to leave the start-up addressing mode.

Hard Disk I/O

The file server will have a built-in Widget hard disk. The interface and controller will be mounted on the same PC board as the processor. The hard disk is accessed via a high-speed parallel interface is defined as follows:

Function	Address	
Data Port w/o PSTRB	500001	
Data Port w/ PSTRB	500003	
Read BSY	500005	read
Reset CMD	500005	write
Reserved	500007	read
Set CMD	500007	write
Read CMD	500009	read
Reset R/W	500009	write
Read R/W	50000B	read
Set R/W	50000B	write
Read INT	50000D	read
Clear Disk Interrupt	50000D	write
Read Timer	50000F	read
Reserved	50000F	write

External Parallel Port Interface

The file server may have (?) an external paralle interface for a ProFile or Widget hard disk drive, or controller for a large disk drive. The interface high-speed parallel interface is defined as follows:

Function	Address	
Data Port w/o PSTRB	580001	
Data Port w/ PSTRB	580003	
Read BSY	580005	read
Reset CMD	580005	write
Reserved	580007	read
Set CMD	580007	write
Read CMD	580009	read
Reset R/W	580009	write
Read R/W	58000B	read
Set R/W	58000B	write
Read INT	58000D	read
Clear Disk Interrupt	58000D	write
Read OCD	58000F	read
Reserved	58000F	write

Time-of-Day Clock

The file server will use a MAC TOD clock chip to provide time and date information to the file server. This clock is battery backed-up, but this feature can be deleted, if desired. Clock addresses are as follows:

Function	Address	
Chip enable	68000x	from SCC DTRB
Clock	68000x	from SCC access
Data from Clock	68000x	to SCC DCDB
Data to Clock	50000x	from int par port R/W

Serial Port I/O

The serial I/O is provided for by an SSC chip and misc logic. The two serial ports will look like Lisa serial ports. One will contain additional control line for modems and the other will be a minimum port that can be used for AppleBus. Refer to the SCC and AppleBus specifications for more information.

Function	Address
SCC	68000x

Timer

A 2ms interrupt is provided. This interrupt must be cleared in the timer interrupt handler by accessing the timer address.

Function	Address
Clear Timer interrupt	480000

Interrupts

There are several sources of the interrupts in the file server. There are channelled down to three levels when they enter the 68000.

Device(s)	Level
SCC & NMI button	4 - 7
Parrallel Ports	2 - 3
2ms Timer	1

Power Supply

The Astec AC 8151 power supply will be used to supply power to the Atlas File Server. The AC 8151 is rated at 40 watts.

Voltage	Current
+5	2.5A
+12	2.0A
-12	0.1A

Note that the maximum load on +5 is specified at 5A when there is no load on the +12v supply.